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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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*Ex parte* VIDYUT GOPAL, SHANKAR SINHA,
JEAN YEE-MEI YANG, and PHILLIP L. JONES

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Appeal 2011-007558
Application 11/724,725
Technology Center 2800

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Before DEBORAH KATZ, JOHN G. NEW, and HUNG H. BUI,
*Administrative Patent Judges*.

BUI, *Administrative Patent Judge.*

DECISION ON APPEAL

Appellants[1] seek our review under 35 U.S.C. § 134(a) of the Examiner's final rejections of claims 1, 3, 5, 6, 8, 9, 11-13, 15, and 16.[2] We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.[3]

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[1] The real party of interest is GlobalFoundries, Inc.

[2] Claims 2, 4, 7, 10, and 14 have been cancelled; Claims 17-20 have been withdrawn from consideration. As such, claims 2, 4, 7, 10, 14, and 17-20 are not on appeal.

## STATEMENT OF THE CASE

### *Appellants' Invention*

Appellants' invention relates to a method of establishing a dielectric extension in a transistor fabrication to mitigate short channel effects. *See* Spec. 1, ll. 9-11, and Abstract.

### *Claims on Appeal*

Claim 1 is the only independent claim on appeal. Claim 1 is illustrative of Appellants' invention, and is reproduced below:

> 1. A method of implementing dielectric extensions in transistor fabrication, comprising:
>
> patterning a layer of gate electrode material such that passivants accumulate on sidewalls of the patterned layer of gate electrode material using a first etching composition to pattern the layer of gate electrode material in an etching chamber;
>
> *switching the etching composition in situ to a second etching composition* and patterning a layer of gate dielectric material in the etching chamber that underlies the patterned gate electrode material;
>
> where the passivants inhibit patterning portions of the layer of gate dielectric material that underlie the passivants;
>
> removing the passivants to reveal dielectric extensions that extend out into apertures formed by the patterning of the layer of gate electrode material and the layer of gate dielectric material;
>
> implanting dopants into a semiconductor substrate that underlies the patterned layer of gate dielectric material to establish source/drain regions in the substrate, where the dielectric extensions substantially block the dopants such that a channel regions defined between the source/drain regions has a

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[3] Our decision refers to Appellants' Appeal Brief filed September 7, 2010 ("App. Br."); Reply Brief filed January 24, 2011 ("Reply Br."); Examiner's Answer mailed November 24, 2010 ("Ans."); and the original Specification filed March 16, 2007 ("Spec.").

length that is greater than a channel length if the dielectric extensions were not present to block the dopants.

*Evidence Considered*

| | | |
|---|---|---|
| Pradeep et al. (Pradeep) | US 5,866,448 | Feb. 2, 1999 |
| Chen | US 6,579,812 B2 | June 17, 2003 |
| Han et al. (Han) | US 2008/0076214 A1 | Mar. 27, 2008 |

*Examiner's Rejections*

(1) Claims 1, 3, 6, 8, 9, 11-13, 15, and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Han and Pradeep. Ans. 3-6.

(2) Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Han, Pradeep, and Chen. Ans. 6-7.

*Issues on Appeal*

Based on Appellants' arguments, the dispositive issue on appeal is whether the Examiner erred in rejecting claims 1, 3, 6, 8, 9, 11-13, 15, and 16 under 35 U.S.C. § 103(a) as being unpatentable over Han and Pradeep. In particular, the issue turns on whether the Examiner's proposed modification of Han and Pradeep is improper because the proposed modification would render Han unsatisfactory for its intended purpose. *See* MPEP § 2143.01(V) (citing *In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984)). App. Br. 3-6; Reply Br. 2-5.

ANALYSIS

The Examiner finds Han discloses a method of implementing dielectric extensions in transistor fabrication having all elements of

Appellants' independent claim 1, including "switching from a first dry etching composition to a second dry etch composition." Ans. 4 (citing Han, ¶¶ [0037]-[0038]). The Examiner acknowledges that Han does not disclose "switching the etching composition in situ [from the first etching composition] to the second etching composition" to pattern (etch) a gate dielectric layer. *Id.* The Examiner then finds Pradeep discloses the missing feature, i.e., "a first dry etching composition is switched in situ to a second dry etching composition when patterning dielectric (fig. 2, 40) and gate electrode (26) layers" respectively. *Id.* at 5 (citing Pradeep, col. 4, ll. 17-48; and FIGS. 2-4).

Based on such factual findings, the Examiner concludes that it would have been obvious "to modify the method of Han and switch the etchant composition in situ between the gate electrode and gate dielectric steps for the purpose of effectively etching the gate electrode and gate dielectric layers while reducing the number of chambers needed to fabricate the device, which may reduce cost." *Id.*

Appellants do not dispute the Examiner's findings regarding Han and Pradeep. Rather, Appellants contend the Examiner's proposed modification of Han and Pradeep is improper because the proposed modification would render Han unsatisfactory for its intended purpose. *See* MPEP § 2143.01(V) (citing *In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984)). App. Br. 3-6; Reply Br. 2-5. In particular, Appellants argue:

> Han teaches a method for forming a semiconductor device. In Fig. 3c, Han forms a layer of photoresist 330 over a surface where a gate region is to be formed. Next, Han uses a poly reactive ion etch (RIE) (alleged "first etching composition") to form a gate electrode 106, where the RIE results in sidewall buildup 334 and damaged dielectric regions

> 332 of the dielectric layer overlying the substrate, as shown in Fig. 3b. The photoresist layer 330 is then stripped off, ***after which*** dilute HF (alleged "second etching composition") is used to remove the damaged portions of the gate dielectric 332 as well as the sidewall buildup 334, resulting in the structure shown in Fig. 3e. (*See* Han, par. [0038]). Therefore as explicitly set forth in par. [0038] of Han, ***the photoresist 330 is stripped before the alleged second etching composition (dilute HF) is applied.***
>
> In contrast, Pradeep teaches a method for forming a semiconductor device, wherein a silicon oxide layer 40 is first etched with a gas mixture employing a photoresist 42 as an etch mask, and then a subsequent second etch is used to etch an underlying polysilicon layer 26. (*See* Pradeep, Figs. 2-4, and col. 4, lns. 17-48). Because the photoresist layer mask 42 in Pradeep is encapsulated within a polymer layer 44 formed during the first etch process, the photoresist layer mask 42 can only be removed after both the first and second etches have been carried out. ***Consequently, in contrast* to *Han, the photoresist* 42 *in Pradeep is stripped only after the alleged second etching composition has been applied.*** (*See* Figs. 4-5)

App. Br. 4.

According to Appellants, the stripping of the photoresist 330 before or after the alleged second etching composition, as shown in FIG. 3d of Han, is significant because the removal of the photoresist 330 by the ashing process as described by Han can damage the exposed portions of the gate oxide region 104, resulting in a transistor having an undesired voltage threshold, current leakage, or inoperable altogether. *Id.* at 5. According to Appellants:

> [B]ecause Han's method requires the removal of photoresist between etching a gate and an underlying dielectric layer to avoid damage to the gate oxide 104, and because Pradeep's *in situ* etching does not allow for the removal of photoresist between *in situ* etchants, ***one of ordinary skill in the art would not be motivated to modify Han in view of Pradeep because***

> ***such a modification would likely render Han's device unsatisfactory for its intended purpose, and perhaps even inoperable***.

*Id.* at 5-6.

As evidence of inoperability, Appellants rely on (1) an article entitled *Impact of F Species on Plasma Charge Damage in a RF asher*, by S.Q. Gu, R. Fujimoto and Peter McGrath, 7th International Symposium on Plasma and Process-Induced Damage, Hawai, June 2002, to show how ashing can damage a gate oxide under a poly line, and (2) an explanation from Wikipedia to show how a transistor's voltage threshold varies as a function of the gate oxide thickness and gate oxide permittivity. *See* THRESHOLD VOLTAGE, http://en.wikipedia.org/wiki/Threshold_voltage (last visited Jan. 24, 2011). Reply Br. 3-4.

However, Appellants' arguments are misplaced. Contrary to Appellants' contention, Pradeep is simply cited for disclosing different etching compositions used to etch a gate dielectric layer and a gate electrode layer, i.e., "a first dry etching composition switched in situ to a second drying etching composition when patterning dielectric (fig. 2, 40) and gate electrode (26) layers" respectively. Ans. 4-5 (citing Pradeep, col. 4, ll. 17-48; and FIGS. 2-4). Such a disclosure is consistent with and complements Han in terms of using different etching compositions to etch a gate dielectric layer and a gate electrode layer on a substrate, as shown in FIGS. 3D-3E.

FIG. 3D and FIG. 3E of Han are reproduced below:

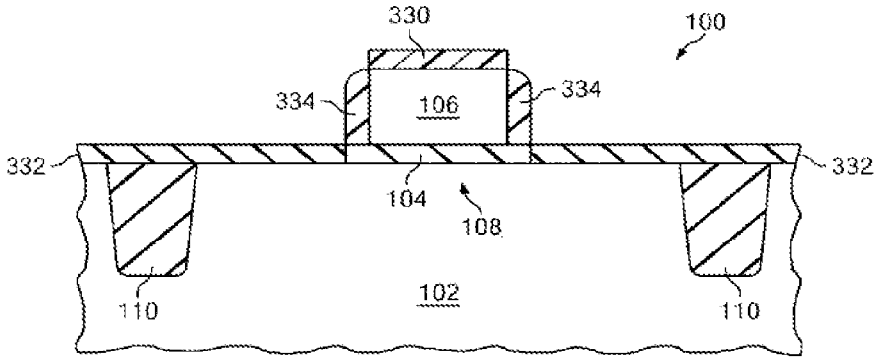


FIG. 3d

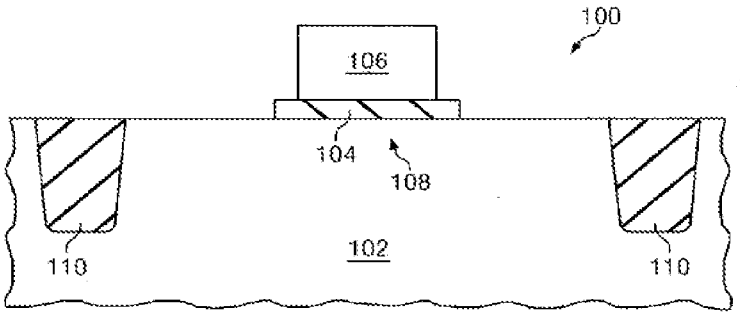


FIG. 3e

FIG. 3D and FIG. 3E depict cross-sectional views of a gate electrode with dielectric extensions of Han

As shown in FIG. 3D of Han, a gate electrode layer 106 is etched, via a conventional poly reactive ion etch (RIE), (i.e., 1st etching composition) such that sidewall build-up 334 (passivants) are accumulated on sidewalls of a gate electrode 106 along with damaged dielectric regions 332. Ans. 4 (citing Han, ¶¶ [0037]-[0038]). Once the gate electrode 106 is etched, hydrofluoric acid (HF) (i.e., 2nd etching composition) is used to remove the sidewall build-up 334 (passivants) as well as the damaged dielectric regions 332, leaving the structure having dielectric extensions shown in FIG. 3E. *Id.* According to Han, different etching techniques with different etching compositions, such as selective wet or dry etch or plasma ashing, can replace the conventional poly reactive ion etch (RIE) and/or hydrofluoric acid (HF)

to etch the gate dielectric layer and the gate electrode layer on a substrate, as shown in FIGS. 3D-3E. *Id.* at 10.

In view of these disclosures, we find incorporating teachings of Pradeep into Han do not alter the timing of when the photoresist 330 is stripped, as shown in FIG. 3D and FIG. 3E of Han, whether before or after the alleged second etching composition, and, likewise, the threshold voltage of MOS transistors. We also find no evidence of alleged inoperability. Neither the article nor the explanation from Wikipedia supports Appellants' contention that the Examiner's proposed modification of Han and Pradeep would not be feasible and would otherwise render Han's device unsatisfactory for its intended purpose. Ans. 8.

Simply, Appellants have not provided us with sufficient reasons to disturb the Examiner's factual findings regarding Han and Pradeep, which are supported by a preponderance of evidence. When a claimed invention "simply arranges old elements with each performing the same function it had been known to perform" and yields no more than one would expect from such an arrangement, the combination is obvious. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 417 (2007) (quoting *Sakraida v. Ag Pro, Inc.*, 425 U.S. 273, 282 (1976)). Appellants do not contest the Examiner's finding that the combination of Han and Pradeep does not yield unexpected results. Ans. 10. As such, we agree with the Examiner's conclusion of obviousness.

For the reasons set forth above, we find no reversible error in the Examiner's position and, as such, sustain the Examiner's obviousness rejection of independent claim 1 over Han and Pradeep.

With respect to dependent claims 3, 5, 6, 8, 9, 11-13, 15, and 16, Appellants present no separate patentability arguments. For the same reasons discussed, we also sustain the Examiner's obviousness rejection of claims 3, 5, 6, 8, 9, 11-13, 15, and 16.

## CONCLUSION

On the record before us, we conclude that the Examiner has not erred in rejecting: (1) claims 1, 3, 6, 8, 9, 11-13, 15, and 16 under 35 U.S.C. § 103(a) as being unpatentable over Han and Pradeep; and (2) claim 5 under 35 U.S.C. § 103(a) as being unpatentable over Han, Pradeep, and Chen.

## DECISION

As such, we AFFIRM the Examiner's final rejections of claims 1, 3, 5, 6, 8, 9, 11-13, 15 and 16.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

## AFFIRMED

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